PRODUCT	MPU	DRAM
$Y_{overall}$	75%	85%
Y_{random}	83%	89.5%
$Y_{systematic}$	90%	95%

Fig. 1

(PRIOR ART)

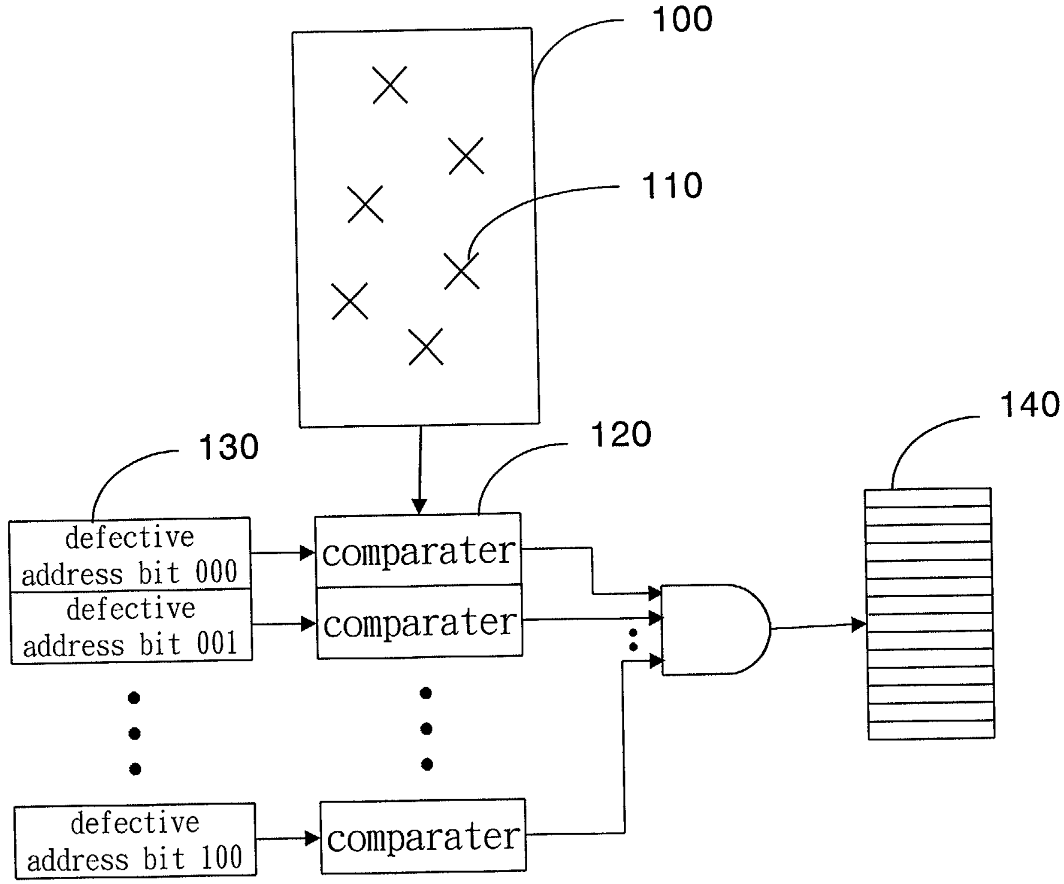

Fig. 2
(PRIOR ART)

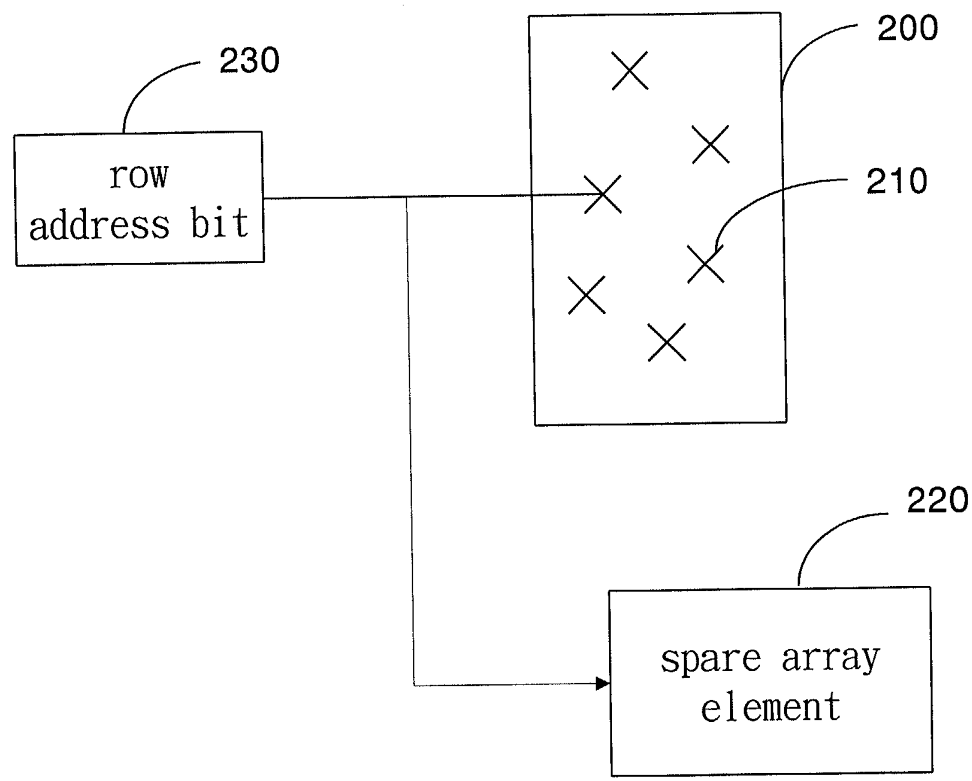

Fig. 3
(PRIOR ART)

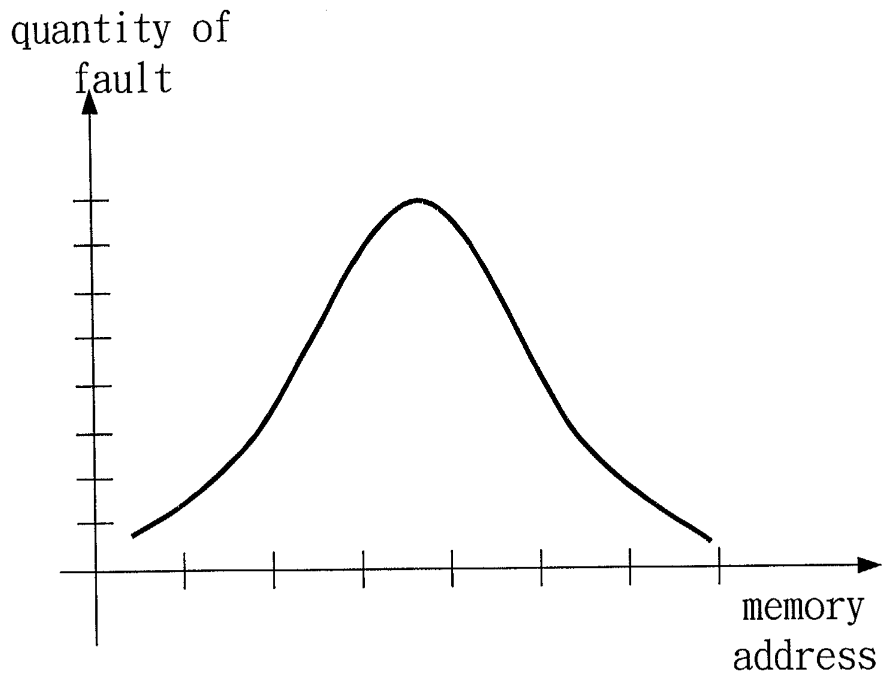

Fig. 4

(PRIOR ART)

a 2G DRAM has 521k memory pages(the size of every memory page is 4k bit)			
every 8k memory pages	every 16k memory pages	every 32k memory pages	every 128k memory pages
Two fault pages are tolerant in every 8k memory pages	Two fault pages in surplus are tolerant in every 16k memory pages	Two fault pages in surplus are tolerant in every 32k memory pages	Four fault pages in surplus are tolerant in every 128k memory pages
Need two associate memories and comparators	Need two associate memories and comparators	Need two associate memories and comparators	Need four associate memories and comparators
There are totally sixty four 8k memory pages in 512k (512/8=64)	There are totally thirty two 16k memory pages in 512k (512/16=32)	There are totally sixteen 32k memory pages in 512k (512/32=16)	There are totally four 128k memory pages in 512k (512/128=4)
128 fault pages are totally tolerant (2*64=128)	64 fault pages are totally tolerant (2*32=64)	32 fault pages are totally tolerant (2*16=32)	16 fault pages are totally tolerant (4*4=16)

Fig. 5

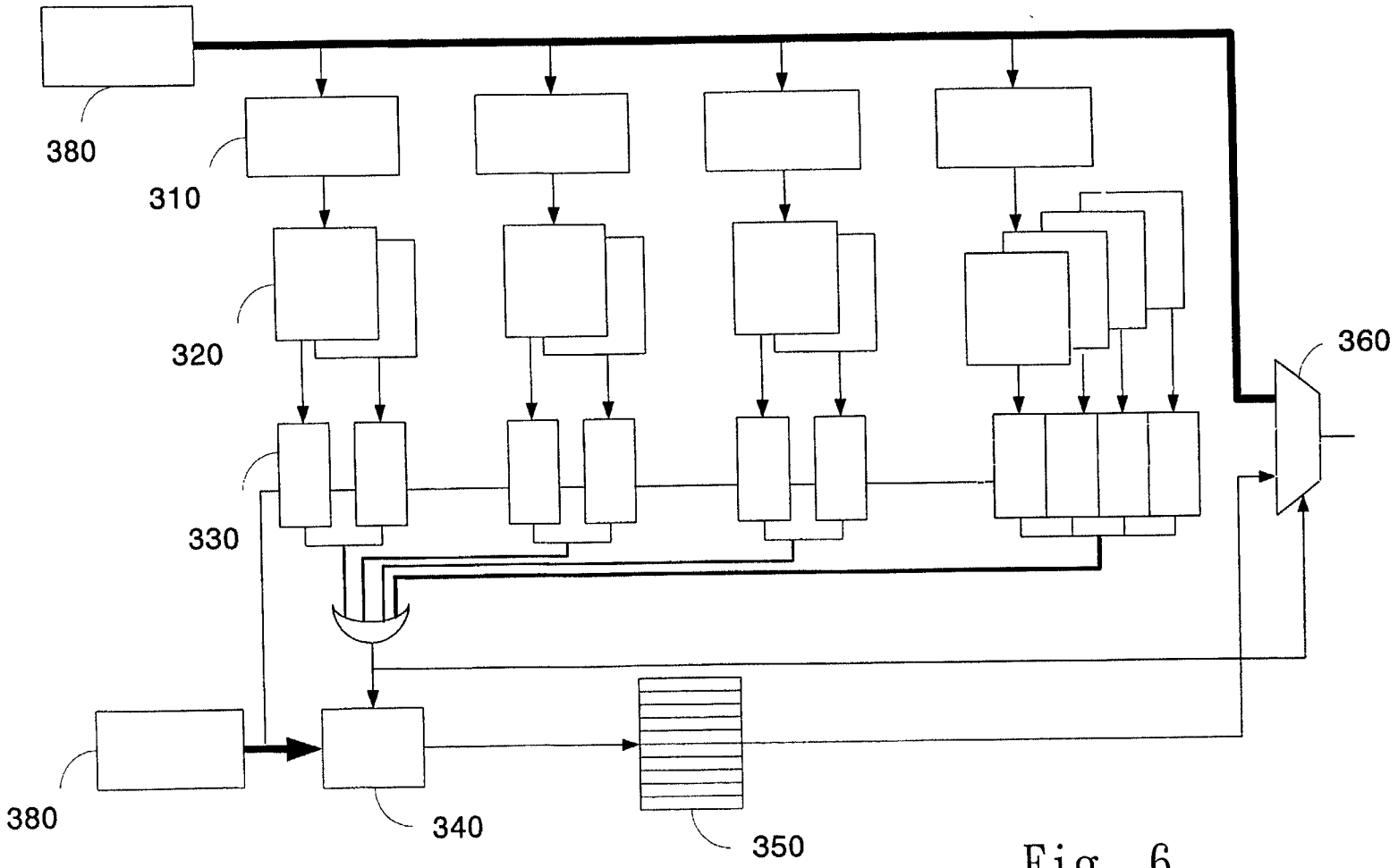

Fig. 6

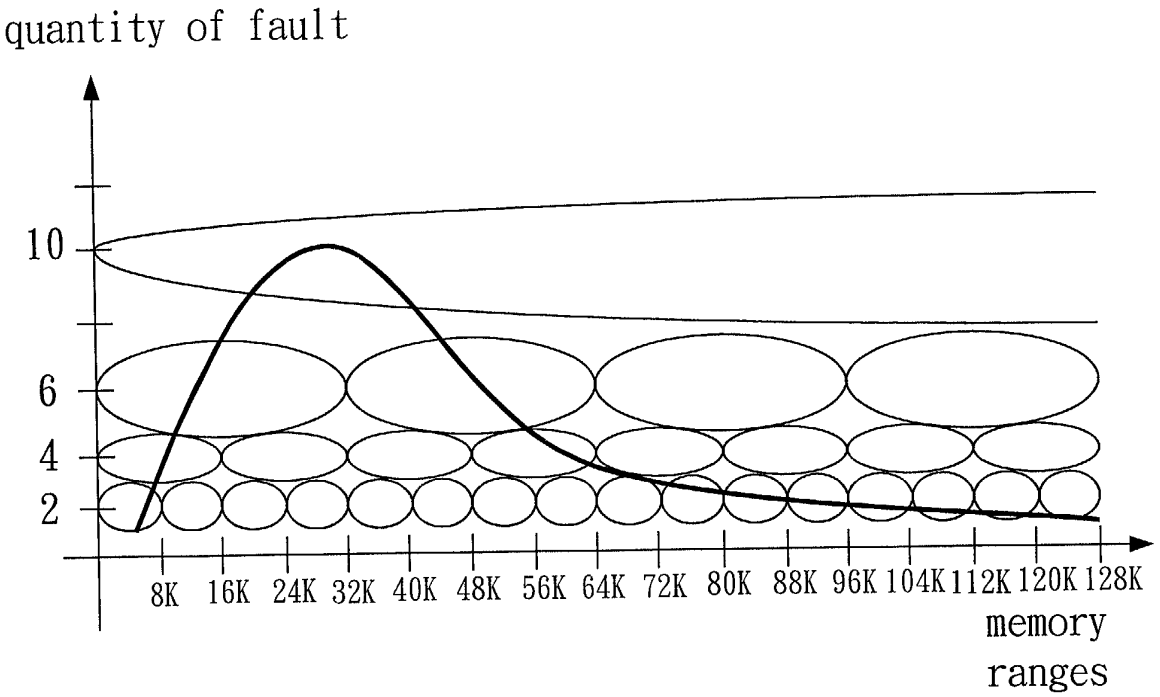
quantity of fault
10
6
4
2
8K
16K
24K
32K
40K
48K
56K
64K
72K
80K
88K
96K
104K
112K
120K
128K
memory
ranges

Fig. 7

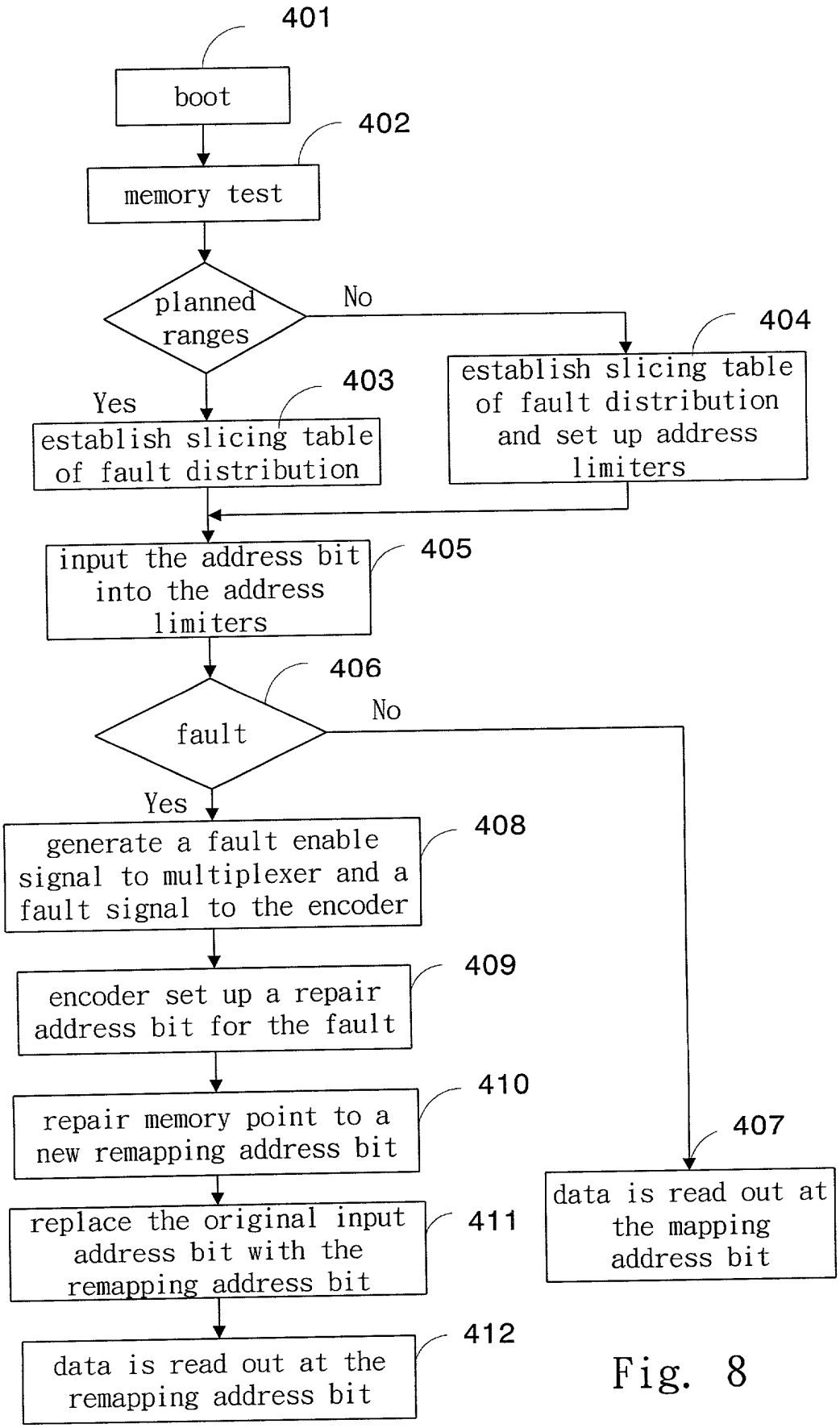
401
boot
402
memory test
planned ranges
No
404
establish slicing table of fault distribution and set up address limiters
Yes
403
establish slicing table of fault distribution
input the address bit into the address limiters
405
406
fault
No
Yes
408
generate a fault enable signal to multiplexer and a fault signal to the encoder
409
encoder set up a repair address bit for the fault
410
repair memory point to a new remapping address bit
411
replace the original input address bit with the remapping address bit
412
data is read out at the remapping address bit
407
data is read out at the mapping address bit

Fig. 8